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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,597	03/10/2004	Xiaobao Wang	015114-054911US	6353

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,597	WANG ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-21,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-11,13-20,23 and 24* is/are rejected.

7)☒ Claim(s) *12 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/4/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

The disclosure is objected to because of the following informalities: Since the parent application, 10/044,365 has become patent, the expression "now Patent No. _____" should follow the filing date of the parent applications in the first sentence of the specification. Appropriate correction is required.

Claim Objections

Claims 6, 11, and 24 are objected to because of the following informalities:

Claim 6, line 6, "an output signal one of" appears to be "an output signal of one of".

Claim 11, line 3, "first transistor and generating" appears to be "first transistor generating" since the first transistor generates analog signal, but not the analog-to-digital converter.

Claim 24, line 3, "resistors" appears to be "resistor".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5-11, 13-20, 23, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu et al. (US 6,445,316 B1, hereinafter, "Hsu").

Regarding claim 1, Hsu discloses, in Figs. 2-4B, an integrated circuit comprising:

a first on-chip impedance termination circuit (280_1) coupled to a first pad (290_1) of the integrated circuit;

a second on-chip impedance termination circuit (280_2) coupled to a second pad (290_2) of the integrated circuit;

a third on-chip impedance termination circuit (280_3) coupled to a third pad (290_3) of the integrated circuit;

a first control circuit (270_1) that adjusts the impedance of the first on-chip impedance termination circuit;

a second control circuit (270_2) that adjusts the impedance of the second on-chip impedance termination circuit independently of the impedance of the first on-chip impedance termination circuit (since 270_2 is separate from 270_1) and

a third control circuit (270_3) that adjusts the impedance of the third on-chip impedance termination circuit independently of the impedance of the first and second on-chip impedance termination circuits (since 270_3 is separate from 270_1 and 270_2).

Regarding claim 3, Hsu discloses, in Figs. 2-4B, an integrated circuit comprising:

a first on-chip impedance termination circuit (280_1) coupled to a first pad (290_1) of the integrated circuit;

a second on-chip impedance termination circuit (280_2) coupled to a second pad (290_2) of the integrated circuit;

a third on-chip impedance termination circuit (280_3) coupled to a third pad (290_3) of the integrated circuit; and

a first control circuit (270_1) that receives a first signal (215) indicative of an off-chip resistance (125; col. 3, line 54+) and a second signal (SELECTOR SIGNAL of 270_1) that indicates an adjusted impedance value for the first pad, the first control circuit adjusting the impedance of the first on-chip impedance termination circuit to a first impedance value in response to the first and the second signals (col. 6, lines 12+);

a second control circuit (270_2) that receives the first signal (215) and a third signal (SELECTOR SIGNAL of 270_2) that indicates an adjusted impedance value for the second pad, the second control circuit adjusting the impedance of the second on-chip impedance termination circuit to a second impedance value in response to the first and the third signals (col. 6, lines 12+); and

a third control circuit (270_3) that receives the first signal (215) and a fourth signal (SELECTOR SIGNAL of 270_3) that indicates an adjusted impedance value for the third pad, the third control circuit adjusting the impedance of the third on-chip impedance termination circuit to a third impedance value in response to the first and the fourth signals (col. 6, lines 12+).

Regarding claim 5, Hsu discloses, in Figs. 2-4B, an integrated circuit comprising:

a digital encoder circuit (340, 360, 350, 370, 310, 320, 330) coupled to receive an analog signal (225) indicative of an impedance of an off-chip resistor (R2; col. 3, lines 54+), the digital encoder circuit generating a plurality of digital signals (PCOMP, NCOMP);

a first bit shifter circuit (270_1)comprising first multiplexers (415, 417) that receive the digital signals, wherein the first multiplexers shift the digital signals to the left in response to a first bit shift signal (SELECTOR SIGNAL=Low) and to the right in response to a second bit shift signal (SELECTOR SIGNAL=High); and

a first impedance termination circuit (280_1) comprising first transistors (287, 288) coupled in parallel and that are each coupled to receive an output signal (DRVCODEP, DRVCODEN) of one of the first multiplexers, each of the first transistors being coupled to a first pin (290_1) of the integrated circuit.

Regarding claim 6, Hsu discloses, in Figs. 2-4B,

a second bit shifter circuit (270_2) comprising second multiplexers (415, 417) that receive the digital signals, wherein the second multiplexers shift the digital signals to the left in response to a third bit shift signal (SELECTOR SIGNAL=Low; see col. 6, lines 49+) and to the right in response to a fourth bit shift signal (SELECTOR SIGNAL=High; see col. 6, lines 49+); and

a second impedance termination circuit (280_2) comprising second transistors (287, 288) coupled in parallel and that are each coupled to receive an output signal (DRVCODEP, DRVCODEN) of one of the second multiplexers, each of the second transistors being coupled to a second pin (290_2) of the integrated circuit.

Regarding claim 7, Hsu discloses, in Figs. 2-4B,

a third bit shifter circuit (270_3) comprising third multiplexers (415, 417) that receive the digital signals, wherein the third multiplexers shift the digital signals to the left in response to a fifth bit shift signal (SELECTOR SIGNAL=Low; see col. 6, lines 49+) and to the right in response to a sixth bit shift signal (SELECTOR SIGNAL=High; see col. 6, lines 49+); and

a third impedance termination circuit (280_3) comprising third transistors (287, 288) coupled in parallel and that are each coupled to receive an output signal (DRVCODEP, DRVCODEN) of one of the third multiplexers, each of the third transistors being coupled to a third pin (290_3) of the integrated circuit.

Regarding claim 8, Hsu discloses, in Figs. 2-4B, that wherein an impedance of the first impedance termination circuit decreases by about ½ in response to the first bit shift signal, and the impedance of the first impedance termination circuit increases by about 2 in response to the second bit shift signal (col. 6, lines 52+)

Regarding claim 9, Hsu discloses, in Figs. 2-4B, that wherein the first impedance termination circuit includes five transistors (287_1-287_5; col. 6, lines 66+) coupled in parallel, the digital encoder circuit generates five digital signal (PCOMP(1)-PCOMP(5)), and the first multiplexers include five multiplexers (415_1-415_5).

Regarding claim 10, Hsu discloses, in Figs. 2-4B, that wherein the first multiplexers receive n digital signals (PCOMP(1)-PCOMP(N)) from the digital encoder circuit and pass each of the n digital signals from the digital encoder circuit to the first transistors (287_1-287_N; col. 6, lines 66+) without bit shifting the n digital signals in response to a bypass signal (SELECTOR SIGNAL=previous state).

Regarding claim 11, Hsu discloses, in Figs. 2-4B, a second on-chip transistor (432, 434 in Fig. 4A) coupled to the off-chip resistor; and an analog-to-digital converter (340, 360, 350, 370) coupled to the first transistor generating the analog signal.

Regarding claim 13, Hsu discloses, in Figs. 2-4B, logic array block (283_1-283_N), each including a plurality of logic elements (AND and OR gate) that are configurable to implement logic functions (AND and OR functions); and a programmable (by 415, 417) interconnect structure (lines connecting 283_1-283_N) connecting the logic array blocks.

Regarding claim 14, Hsu discloses, in Figs. 2-4B, that wherein the first impedance termination circuit (280_1) is coupled to provide parallel termination impedance (see 287_1-287_N and 288_1-288_N) to the first pin (290_1).

Regarding claim 15, Hsu discloses, in Figs. 2-4B, that wherein the first impedance termination circuit (280_1) is coupled to provide series termination impedance (since there are series of transistors 287_1-287_N and 288_1-288_N connected, it can be interpreted as series termination impedance whether or not they are serially connected) to the first pin (290_1).

Method claims 16-20, 23 and 24 are essentially the same in scope as apparatus claims 5, 6, 8, 11, 14 and 15 and are rejected similarly.

Response to Argument

Applicant's arguments with respect to claims 1, 3, 5-21, 23, and 24 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claims 12 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Hsu, taken alone or in combination of other references, does not teach or fairly suggest an integrated circuit comprising, among other things, that wherein the first multiplexers shift the digital signals to the left by two bits in response to a third bit shift signal

and to the right by two bits in response to a fourth bit shift signal (claim 12); and wherein shifting the digital signals by at least one bit to generate bit shifted signals further comprises: shifting the digital signals by two bits to generate the bit shifted signals (claim 21), as set forth in the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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